FIG. 1

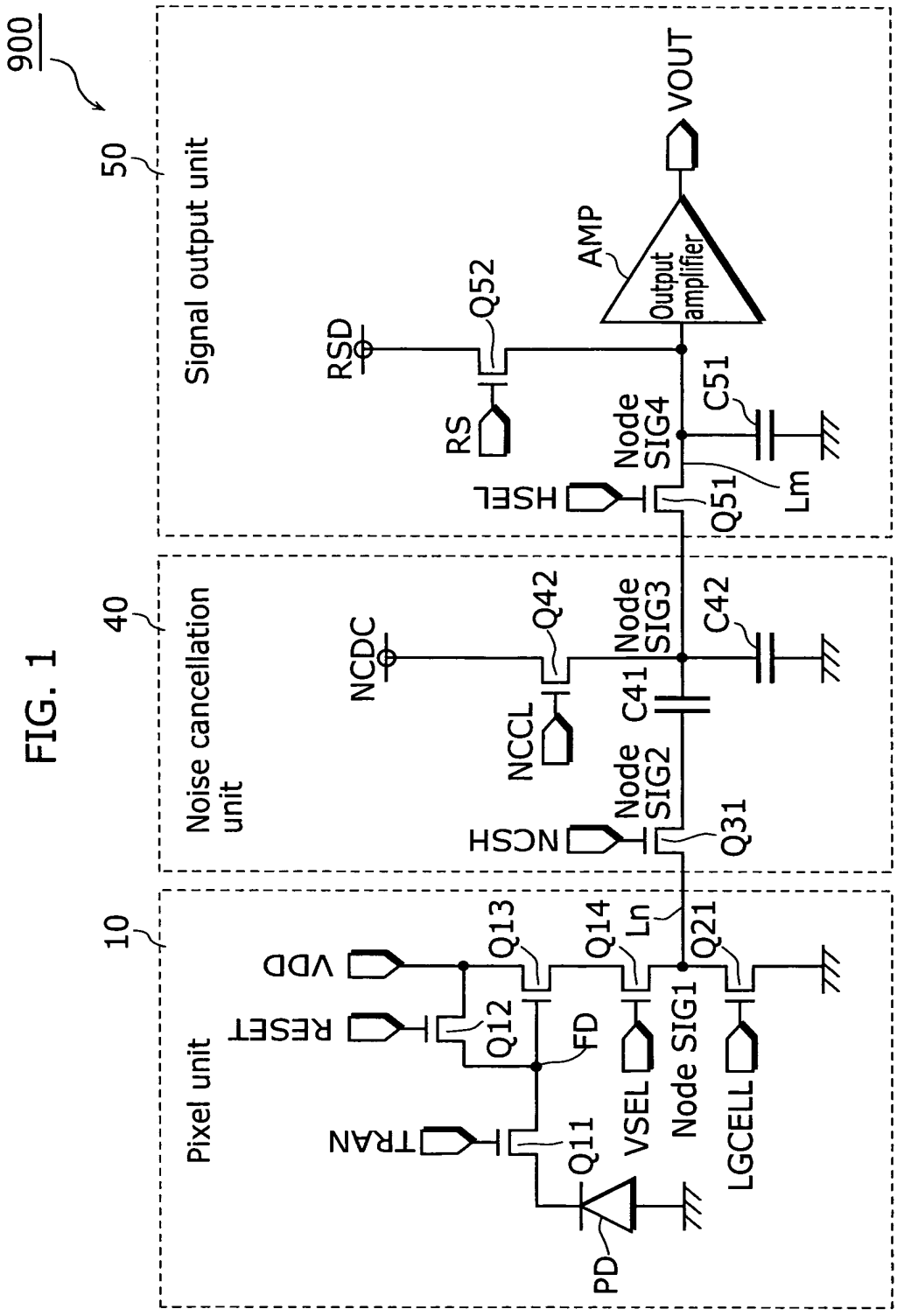

900
10
Pixel unit
40
Noise cancellation unit
50
Signal output unit
VDD
RESET
TRAN
PD
Q11
Q12
Q13
FD
Q14
VSEL
Ln
Node SIG1
Q21
LGCELL
NCSH
Node SIG2
Q31
C41
NCCL
NCDC
Q42
Node SIG3
C42
HSEL
Q51
Lm
Node SIG4
C51
RS
RSD
Q52
AMP
Output amplifier
VOUT

FIG. 2

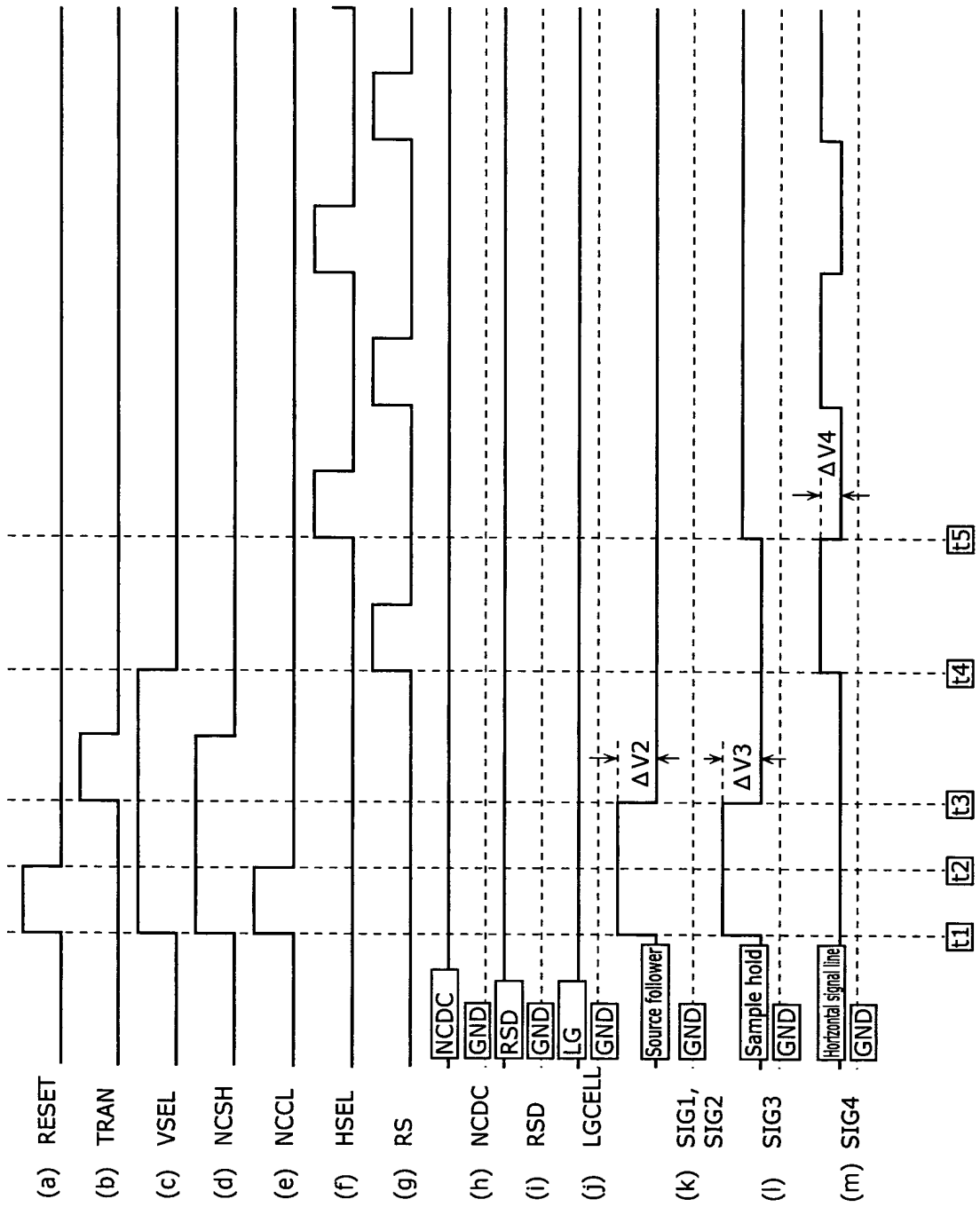

(a) RESET
(b) TRAN
(c) VSEL
(d) NCSH
(e) NCCL
(f) HSEL
(g) RS
(h) NCDC
(i) RSD
(j) LGCELL
(k) SIG1, SIG2
(l) SIG3
(m) SIG4
NCDC
GND
RSD
GND
LG
GND
Source follower
GND
Sample hold
GND
Horizontal signal line
GND
ΔV2
ΔV3
ΔV4
t1
t2
t3
t4
t5

FIG. 3

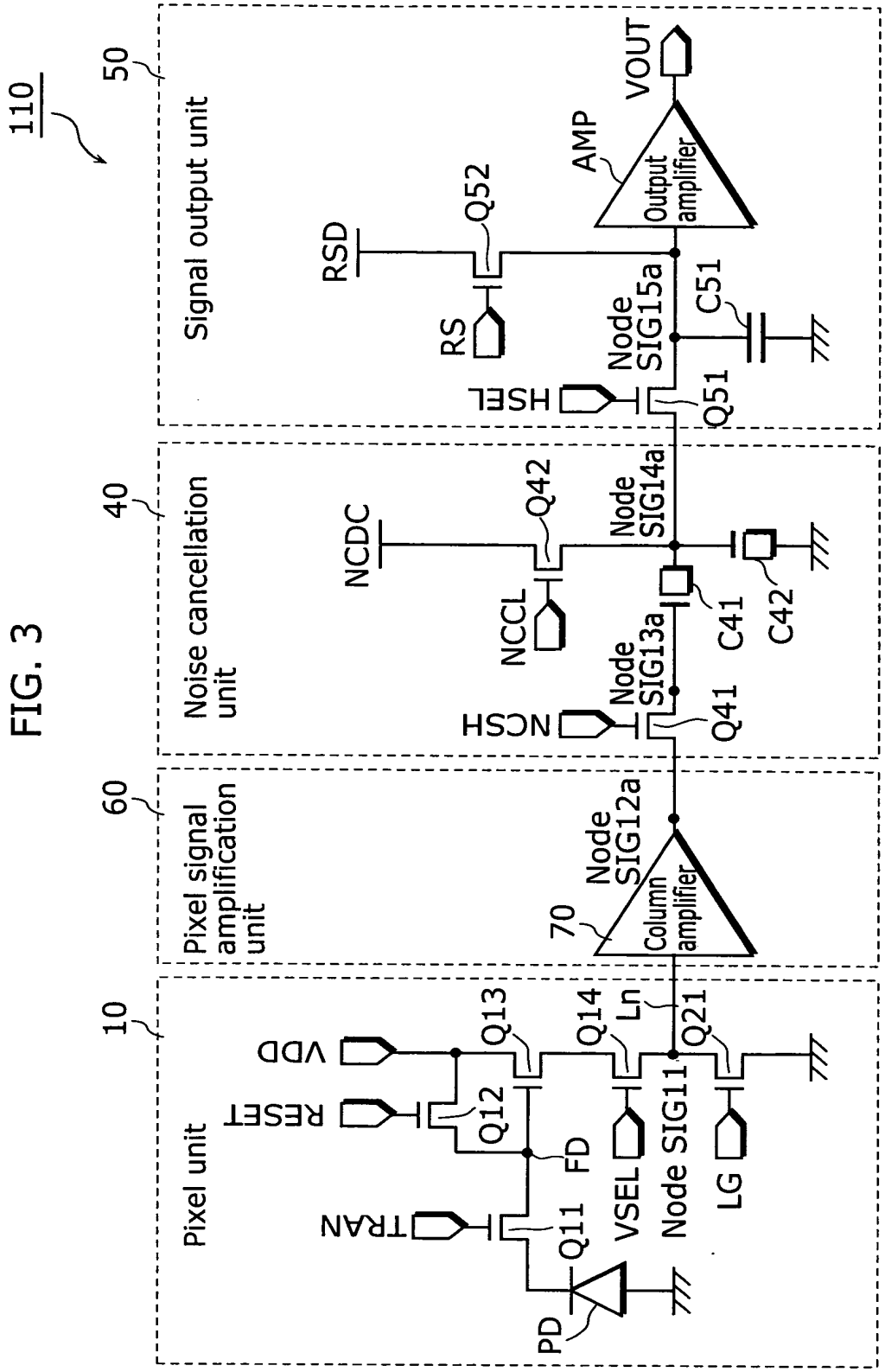

110
10
Pixel unit
PD
Q11
TRAN
FD
Q12
RESET
VDD
Q13
Q14
VSEL
Ln
Node SIG11
Q21
LG
60
Pixel signal amplification unit
70
Column amplifier
Node SIG12a
40
Noise cancellation unit
NCSH
Q41
Node SIG13a
C41
C42
NCCL
Q42
NCDC
Node SIG14a
50
Signal output unit
HSEL
Q51
Node SIG15a
C51
RS
Q52
RSD
AMP
Output amplifier
VOUT

FIG. 4

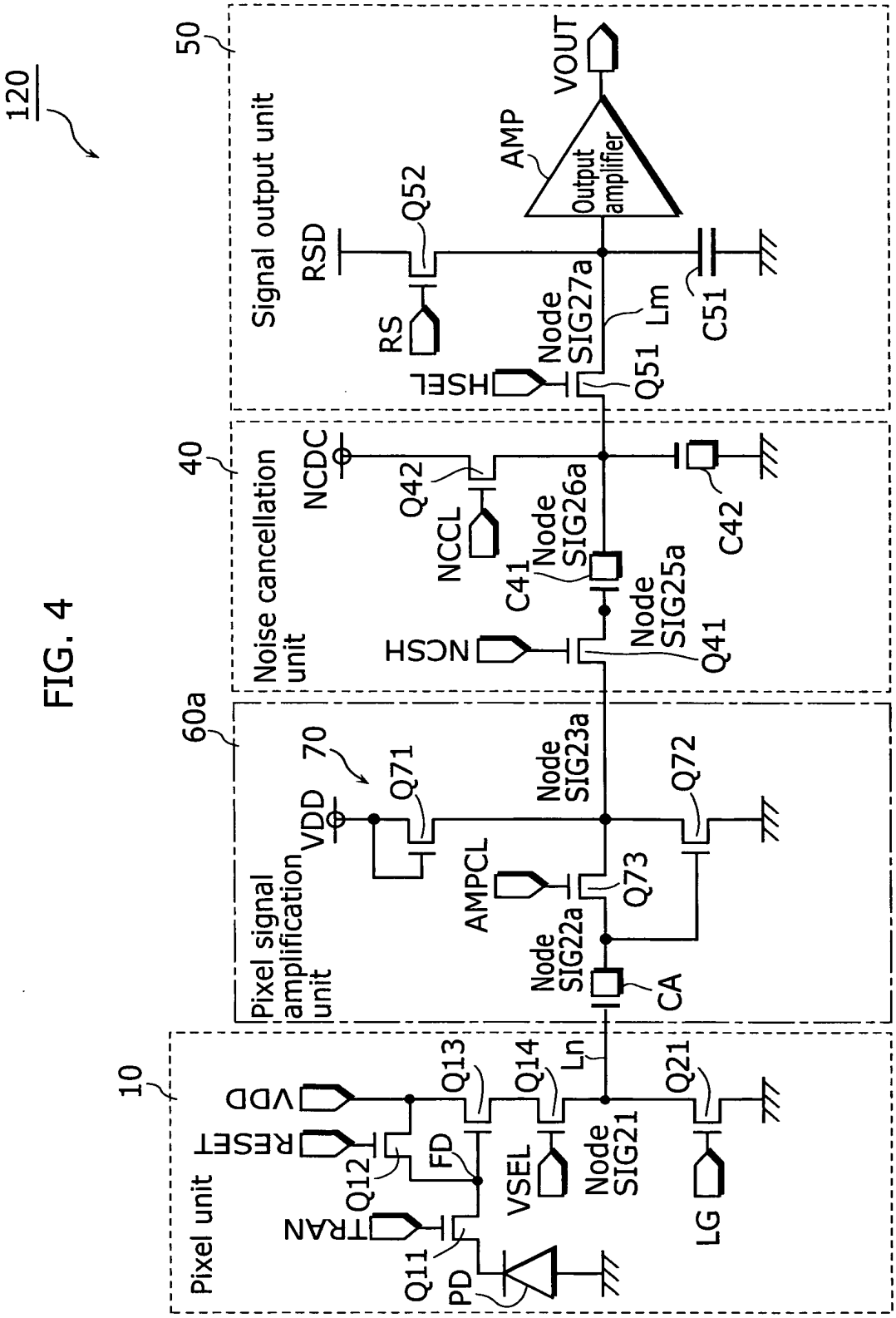

120
50
Signal output unit
VOUT
AMP
Output amplifier
RSD
Q52
RS
HSEL
Node SIG27a
Q51
Lm
C51
40
Noise cancellation unit
NCDC
Q42
NCCL
C41
Node SIG26a
Node SIG25a
NCSH
Q41
C42
60a
Pixel signal amplification unit
70
VDD
Q71
AMPCL
Node SIG23a
Q73
Q72
Node SIG22a
CA
10
Pixel unit
VDD
RESET
Q12
FD
TRAN
Q11
PD
Q13
Q14
VSEL
Ln
Node SIG21
Q21
LG

FIG. 5

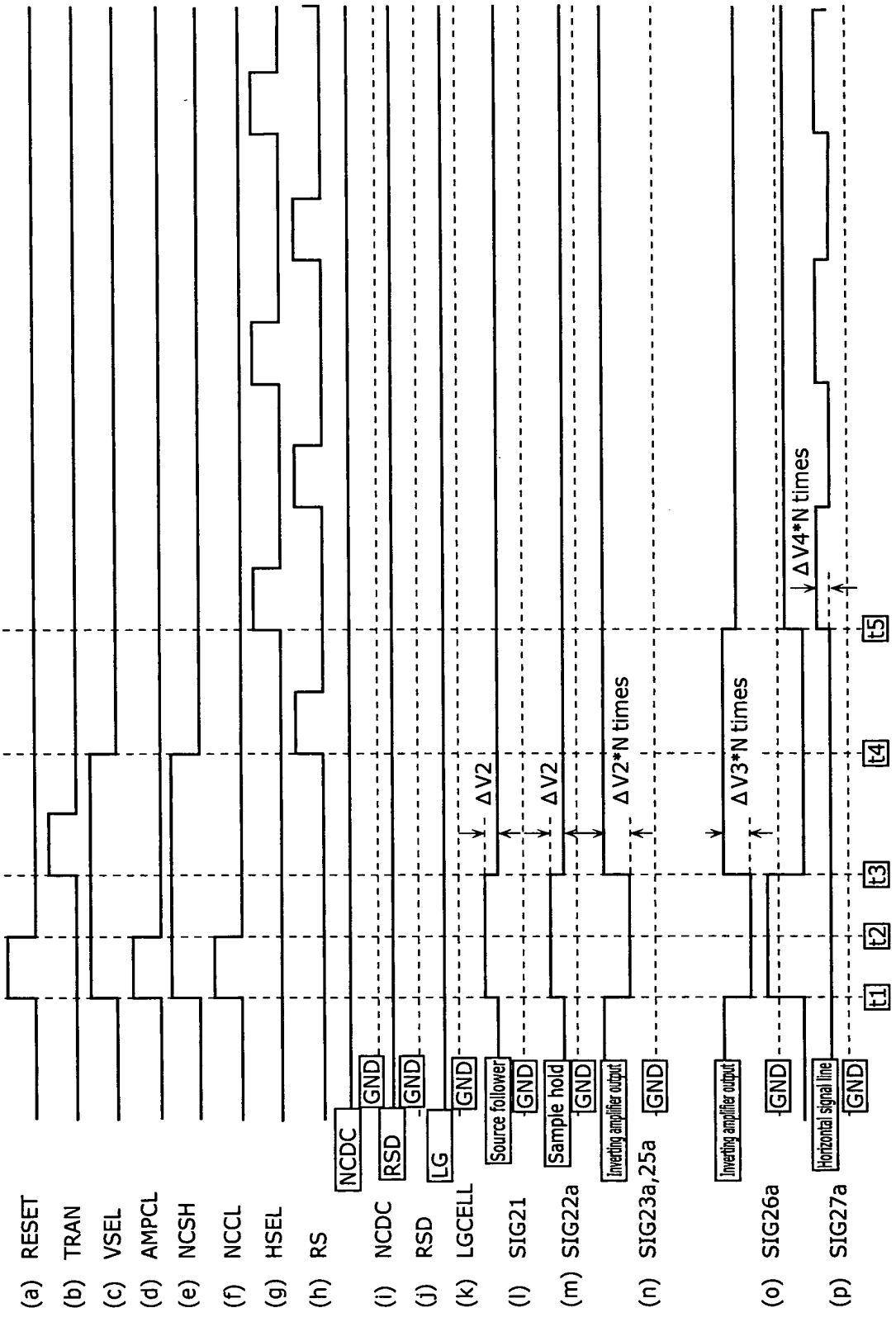

(a) RESET
(b) TRAN
(c) VSEL
(d) AMPCL
(e) NCSH
(f) NCCL
(g) HSEL
(h) RS
(i) NCDC
(j) RSD
(k) LGCELL
(l) SIG21
(m) SIG22a
(n) SIG23a,25a
(o) SIG26a
(p) SIG27a
NCDC
RSD
LG
GND
Source follower
Sample hold
Inverting amplifier output
Horizontal signal line
ΔV2
ΔV2*N times
ΔV3*N times
ΔV4*N times
t1
t2
t3
t4
t5

FIG. 6

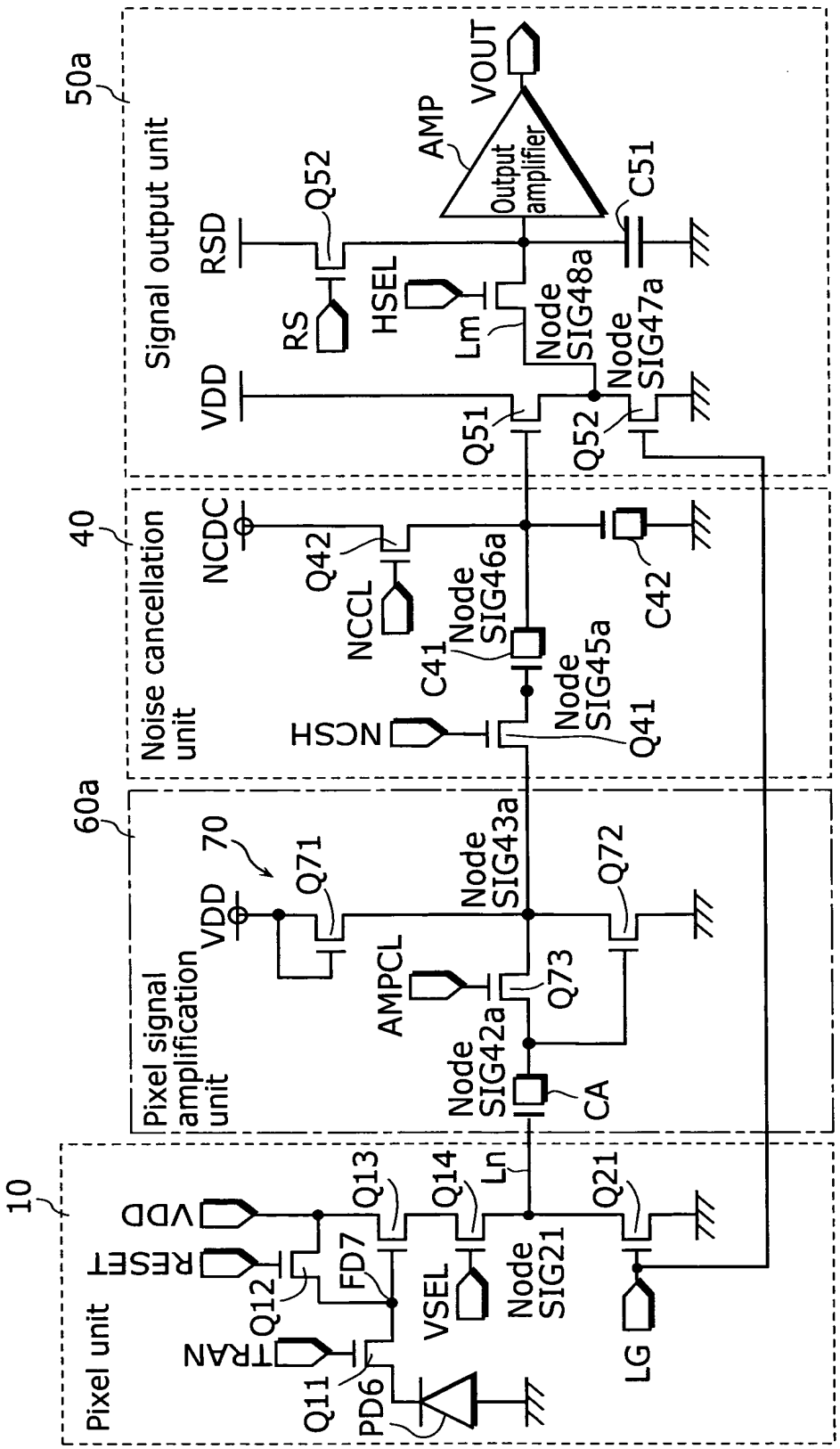

130
10
Pixel unit
VDD
RESET
TRAN
Q12
FD7
Q13
Q14
Ln
VSEL
Node SIG21
Q21
LG
Q11
PD6
60a
Pixel signal amplification unit
VDD
70
Q71
Node SIG43a
Q72
AMPCL
Q73
Node SIG42a
CA
40
Noise cancellation unit
NCDC
Q42
NCCL
Node SIG46a
C41
NCSH
Node SIG45a
Q41
C42
50a
Signal output unit
RSD
Q52
RS
HSEL
Lm
Node SIG48a
AMP
Output amplifier
VOUT
C51
VDD
Q51
Q52
Node SIG47a

FIG. 7

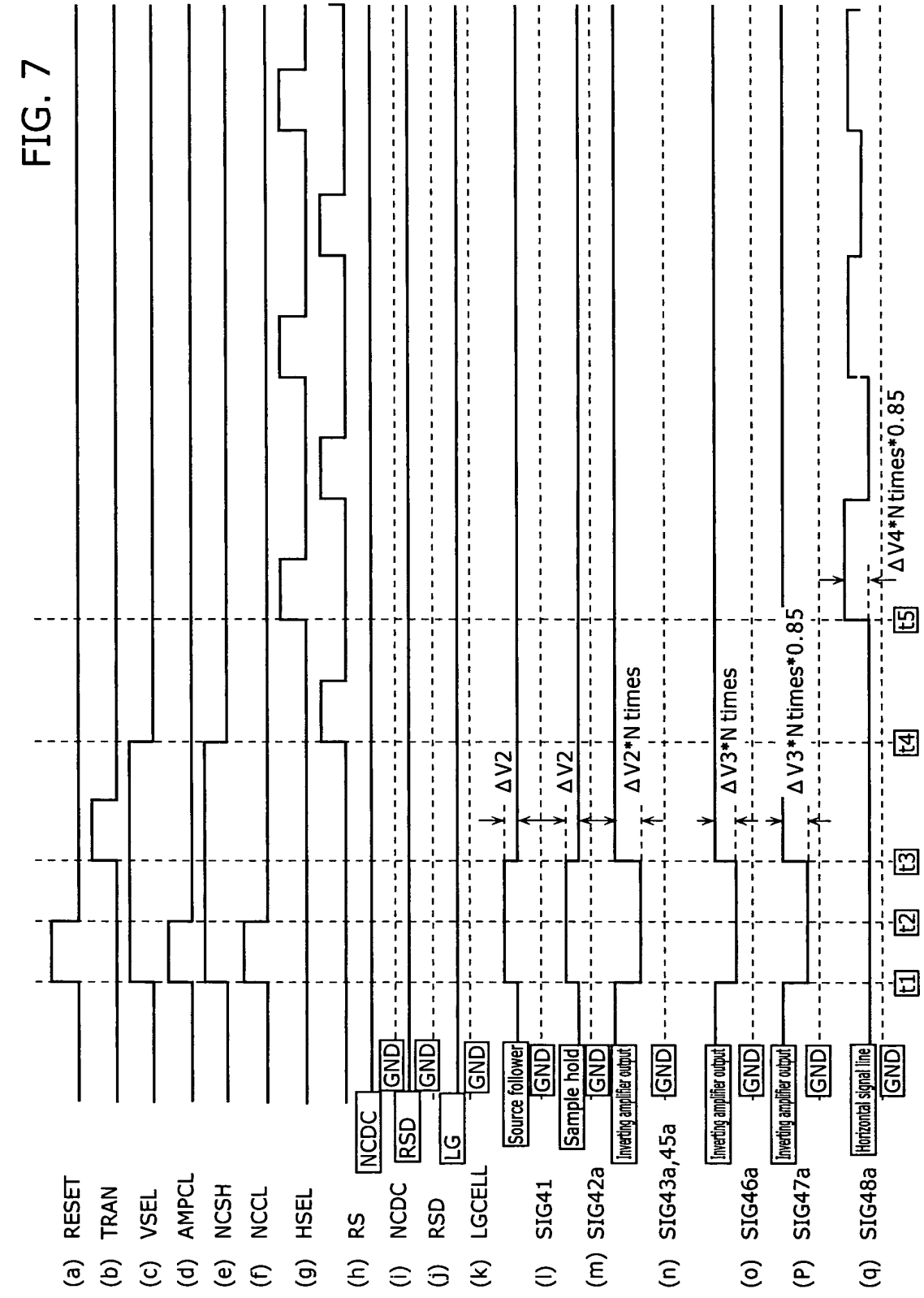

(a) RESET
(b) TRAN
(c) VSEL
(d) AMPCL
(e) NCSH
(f) NCCL
(g) HSEL
(h) RS
(i) NCDC
(j) RSD
(k) LGCELL
(l) SIG41
(m) SIG42a
(n) SIG43a,45a
(o) SIG46a
(P) SIG47a
(q) SIG48a
NCDC
GND
RSD
GND
LG
GND
Source follower
GND
Sample hold
GND
Inverting amplifier output
GND
Inverting amplifier output
GND
Inverting amplifier output
GND
Horizontal signal line
GND
ΔV2
ΔV2
ΔV2*N times
ΔV3*N times
ΔV3*N times*0.85
ΔV4*N times*0.85
t1
t2
t3
t4
t5

FIG. 8

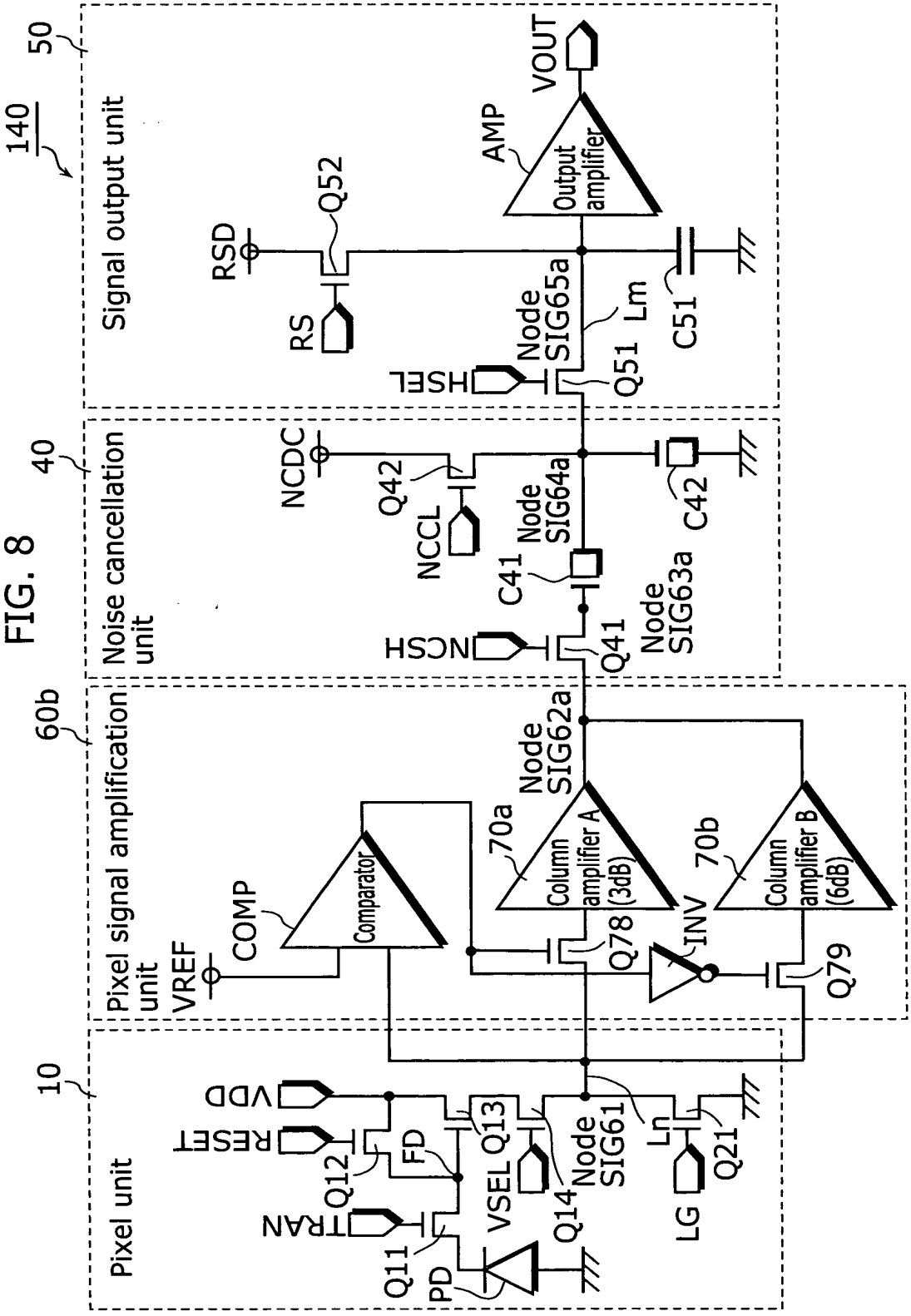

140
50
Signal output unit
40
Noise cancellation unit
60b
Pixel signal amplification unit
10
Pixel unit
VOUT
AMP
Output amplifier
RSD
Q52
RS
HSEL
Node SIG65a
Lm
Q51
C51
NCDC
Q42
NCCL
Node SIG64a
C42
C41
NCSH
Q41
Node SIG63a
Node SIG62a
VREF
COMP
Comparator
70a
Column amplifier A (3dB)
70b
Column amplifier B (6dB)
INV
Q78
Q79
VDD
RESET
Q12
FD
Q13
TRAN
Q11
PD
VSEL
Q14
Node SIG61
Ln
Q21
LG

FIG. 9

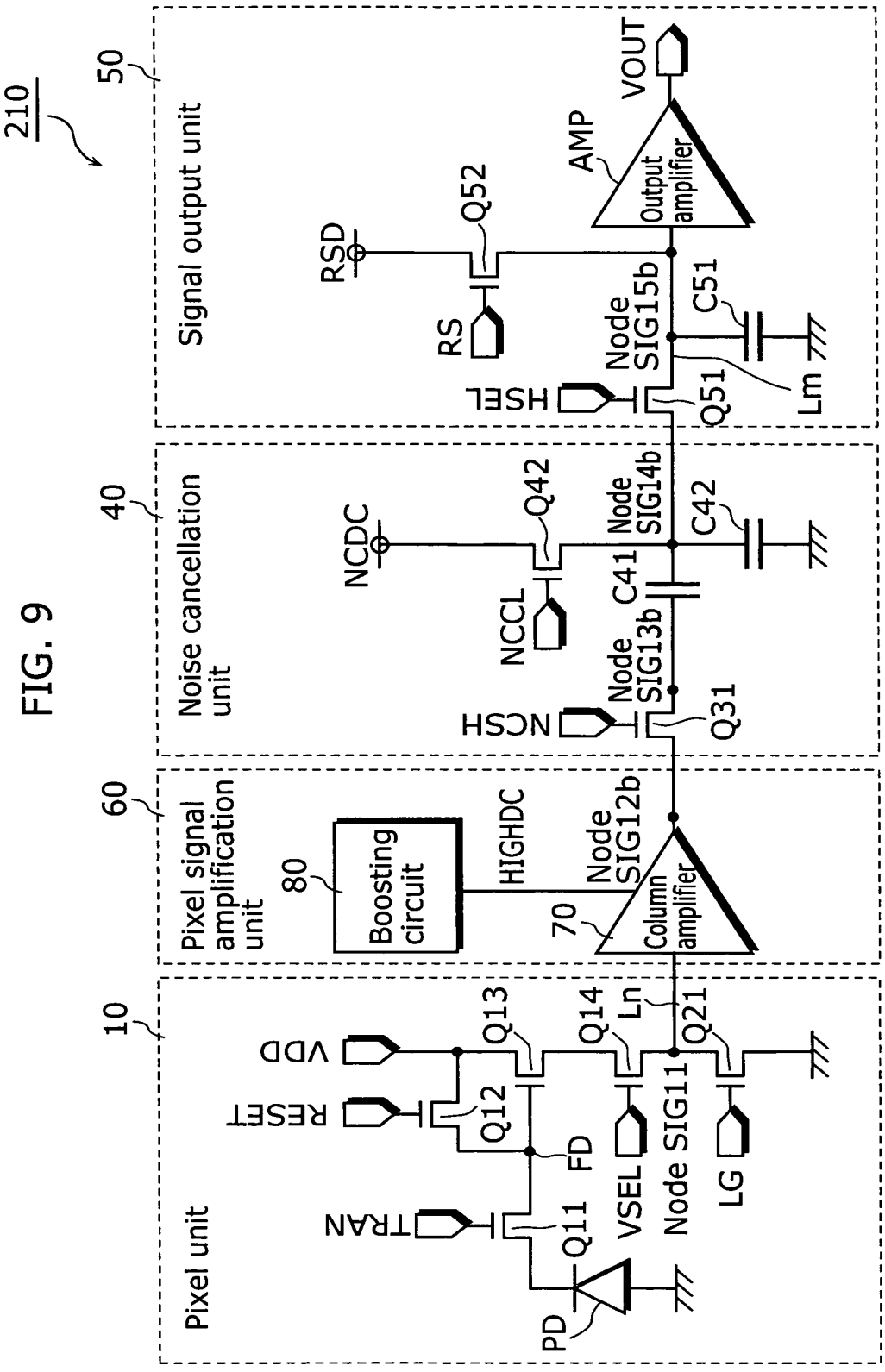

210
10
Pixel unit
PD
Q11
TRAN
FD
Q12
RESET
VDD
Q13
Q14
Ln
VSEL
Node SIG11
Q21
LG
60
Pixel signal amplification unit
80
Boosting circuit
HIGHDC
Node SIG12b
70
Column amplifier
40
Noise cancellation unit
NCSH
Q31
Node SIG13b
C41
NCCL
Q42
NCDC
Node SIG14b
C42
50
Signal output unit
Q51
Lm
HSEL
Node SIG15b
C51
RS
Q52
RSD
AMP
Output amplifier
VOUT

FIG. 10

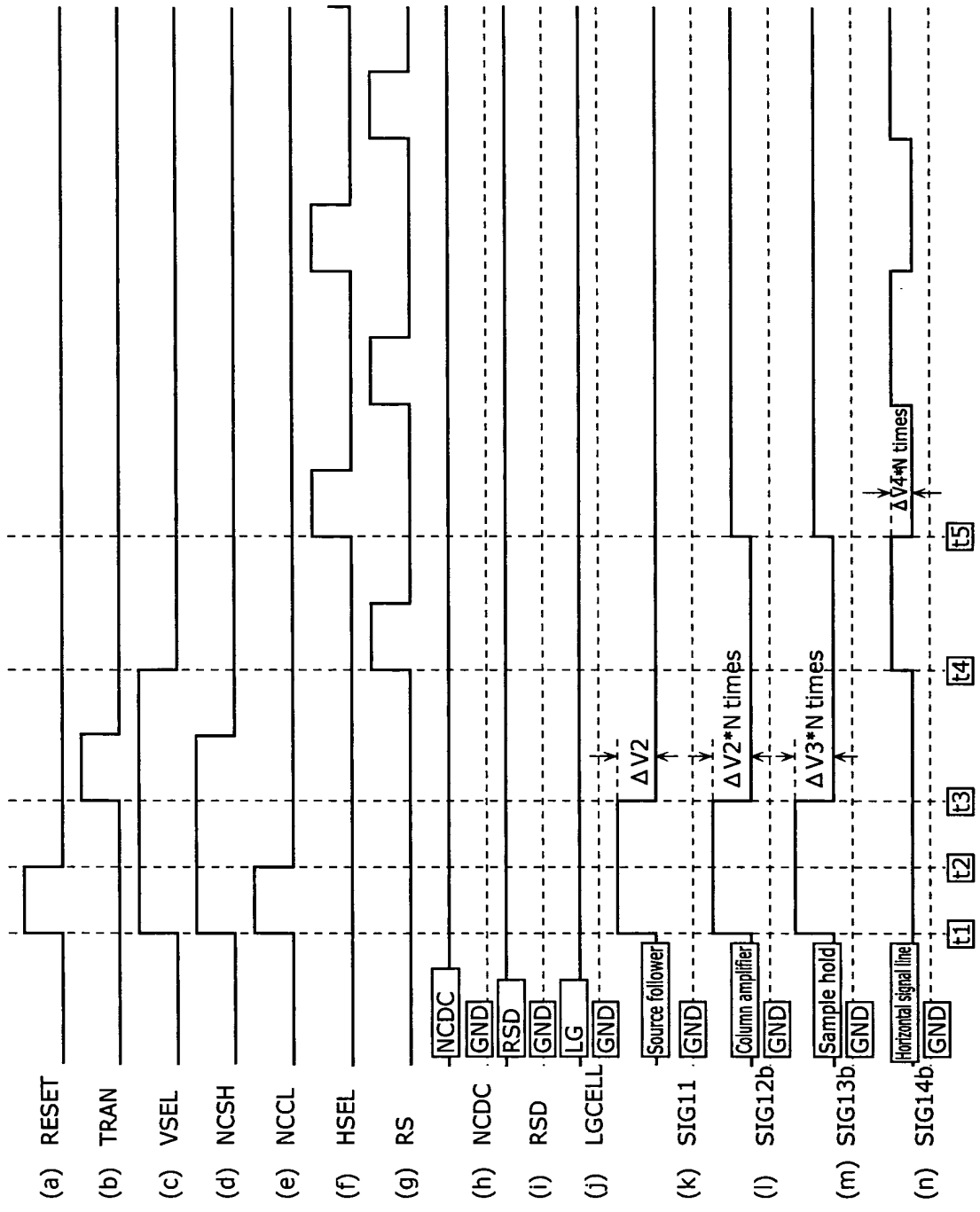

(a) RESET
(b) TRAN
(c) VSEL
(d) NCSH
(e) NCCL
(f) HSEL
(g) RS
(h) NCDC
(i) RSD
(j) LGCELL
(k) SIG11
(l) SIG12b
(m) SIG13b
(n) SIG14b
NCDC
GND
RSD
GND
LG
GND
ΔV2
Source follower
GND
ΔV2*N times
Column amplifier
GND
ΔV3*N times
Sample hold
GND
ΔV4*N times
Horizontal signal line
GND
t1
t2
t3
t4
t5

FIG. 11

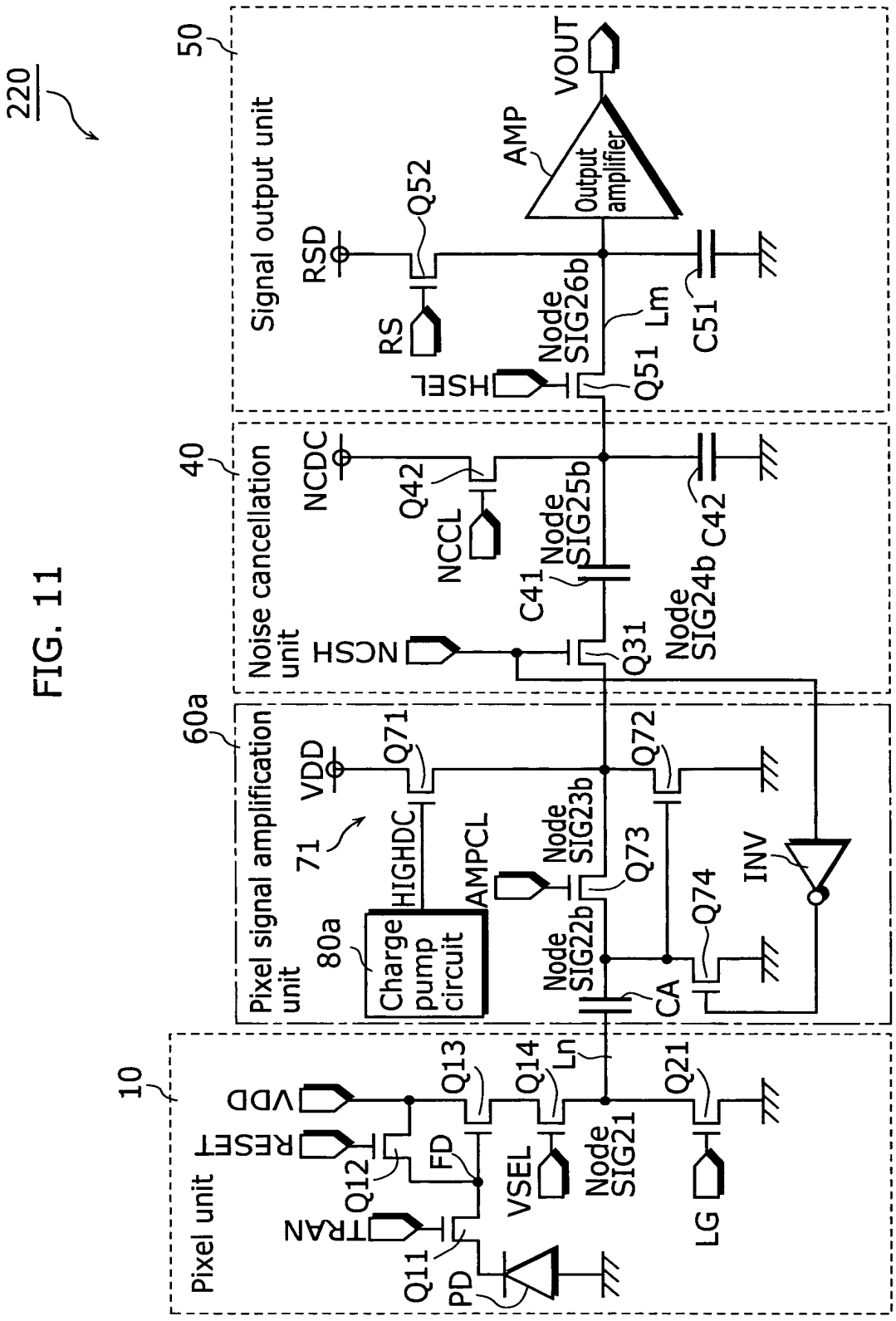

220
10
Pixel unit
VDD
RESET
TRAN
Q11
PD
Q12
FD
Q13
VSEL
Q14
Ln
Node SIG21
Q21
LG
60a
Pixel signal amplification unit
VDD
Q71
71
HIGHDC
80a
Charge pump circuit
AMPCL
Node SIG23b
Q72
Q73
Node SIG22b
CA
Q74
INV
40
Noise cancellation unit
NCSH
Q31
C41
Node SIG25b
NCCL
Q42
NCDC
Node SIG24b
C42
50
Signal output unit
HSEL
Q51
Node SIG26b
Lm
RS
Q52
RSD
C51
AMP
Output amplifier
VOUT

FIG. 12

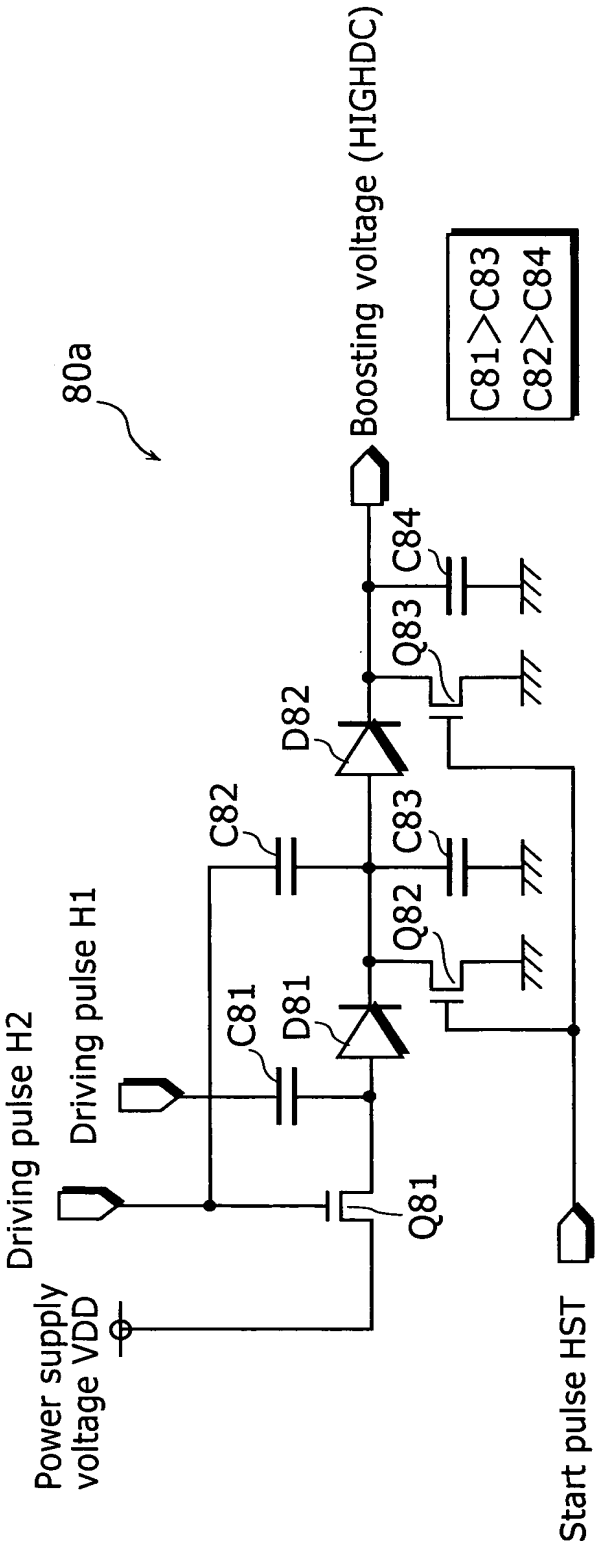

80a
Boosting voltage (HIGHDC)
C81>C83
C82>C84
C84
Q83
D82
C82
C83
Q82
C81
D81
Q81
Driving pulse H2
Driving pulse H1
Power supply voltage VDD
Start pulse HST

FIG. 13

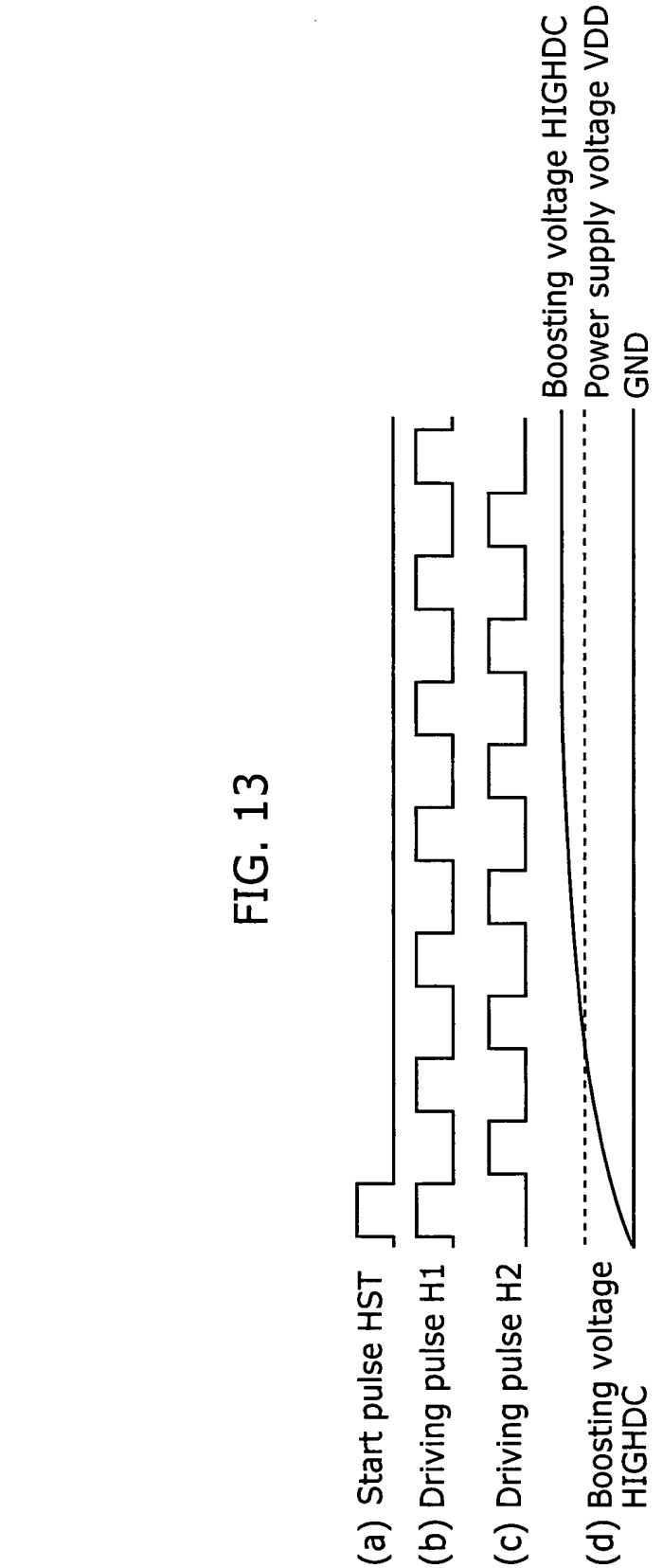

(a) Start pulse HST
(b) Driving pulse H1
(c) Driving pulse H2
(d) Boosting voltage HIGHDC
Boosting voltage HIGHDC
Power supply voltage VDD
GND

FIG. 14

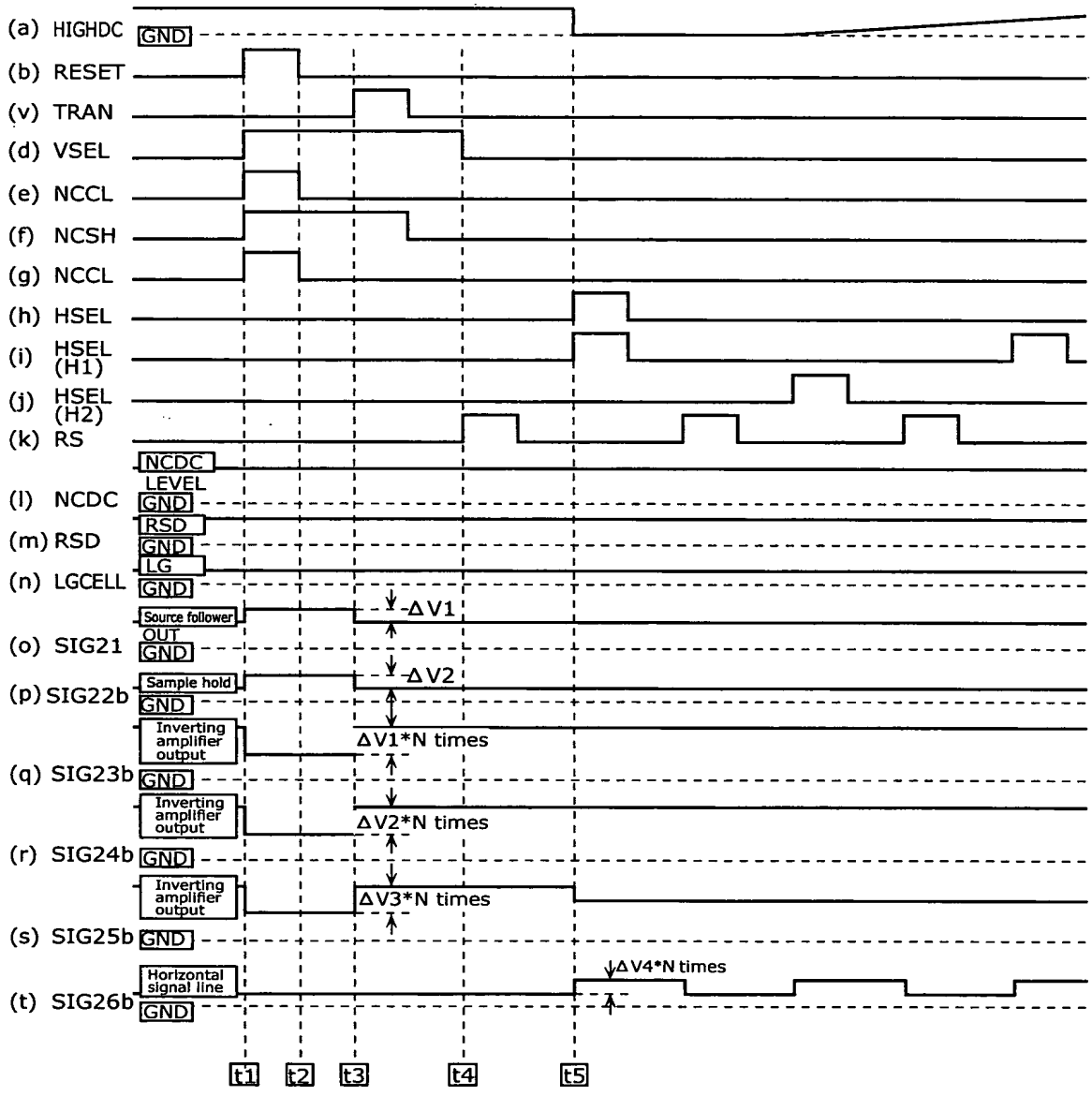

(a) HIGHDC
GND
(b) RESET
(v) TRAN
(d) VSEL
(e) NCCL
(f) NCSH
(g) NCCL
(h) HSEL
(i) HSEL (H1)
(j) HSEL (H2)
(k) RS
NCDC LEVEL
(l) NCDC
GND
RSD
(m) RSD
GND
LG
(n) LGCELL
GND
Source follower
-ΔV1
OUT
(o) SIG21
GND
Sample hold
-ΔV2
(p) SIG22b
GND
Inverting amplifier output
ΔV1*N times
(q) SIG23b
GND
Inverting amplifier output
ΔV2*N times
(r) SIG24b
GND
Inverting amplifier output
ΔV3*N times
(s) SIG25b
GND
Horizontal signal line
ΔV4*N times
(t) SIG26b
GND
t1
t2
t3
t4
t5

FIG. 15

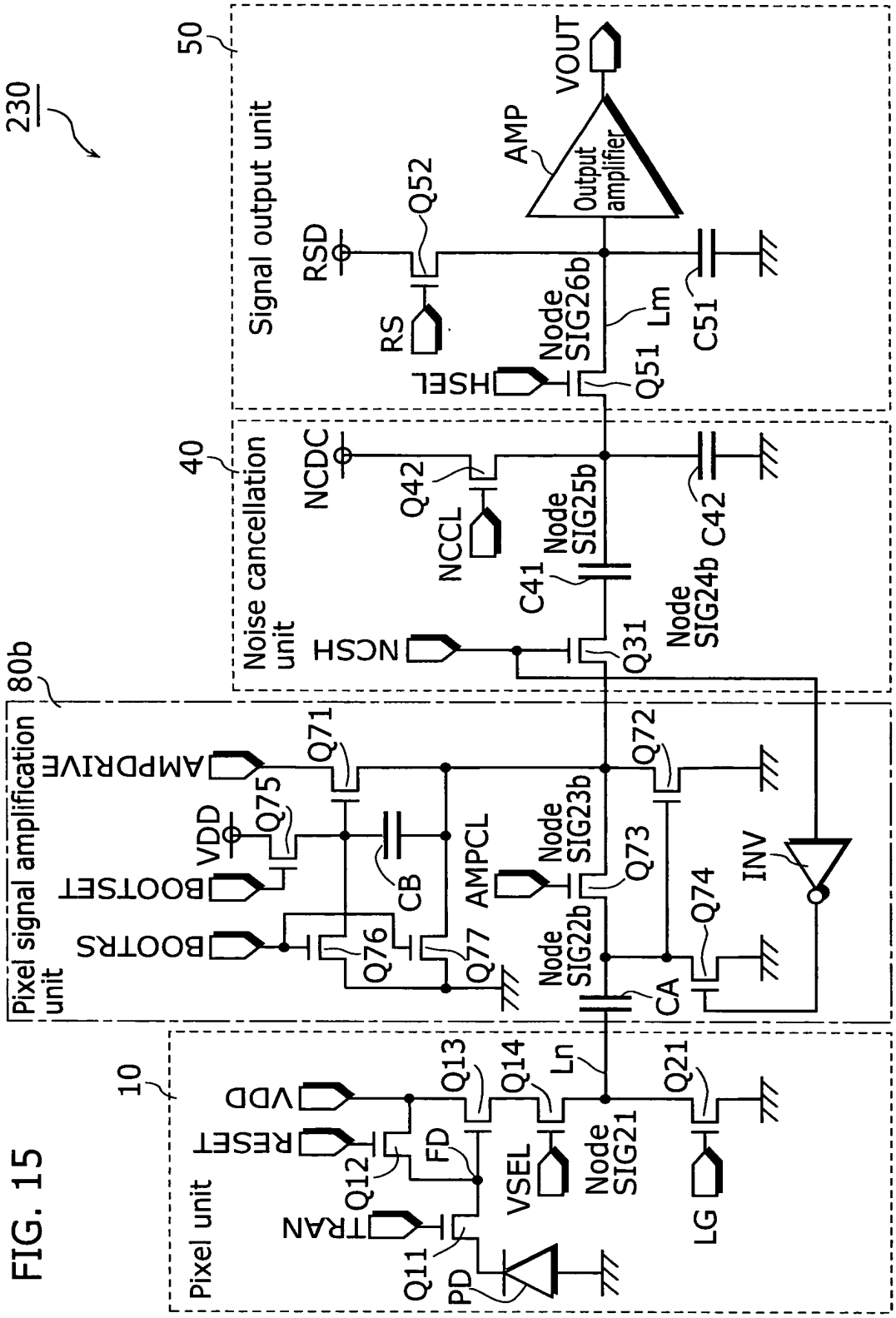

230
50
Signal output unit
VOUT
AMP
Output amplifier
RSD
Q52
RS
HSEL
Node SIG26b
Q51
Lm
C51
40
Noise cancellation unit
NCDC
Q42
NCCL
C41
Node SIG25b
C42
Node SIG24b
NCSH
Q31
80b
Pixel signal amplification unit
AMPDRIVE
Q71
Q72
VDD
Q75
BOOTSET
BOOTRS
CB
Q76
Q77
AMPCL
Node SIG23b
Q73
Node SIG22b
CA
Q74
INV
10
Pixel unit
VDD
Q13
Q14
Ln
Q21
RESET
Q12
FD
VSEL
Node SIG21
TRAN
Q11
PD
LG

FIG. 16

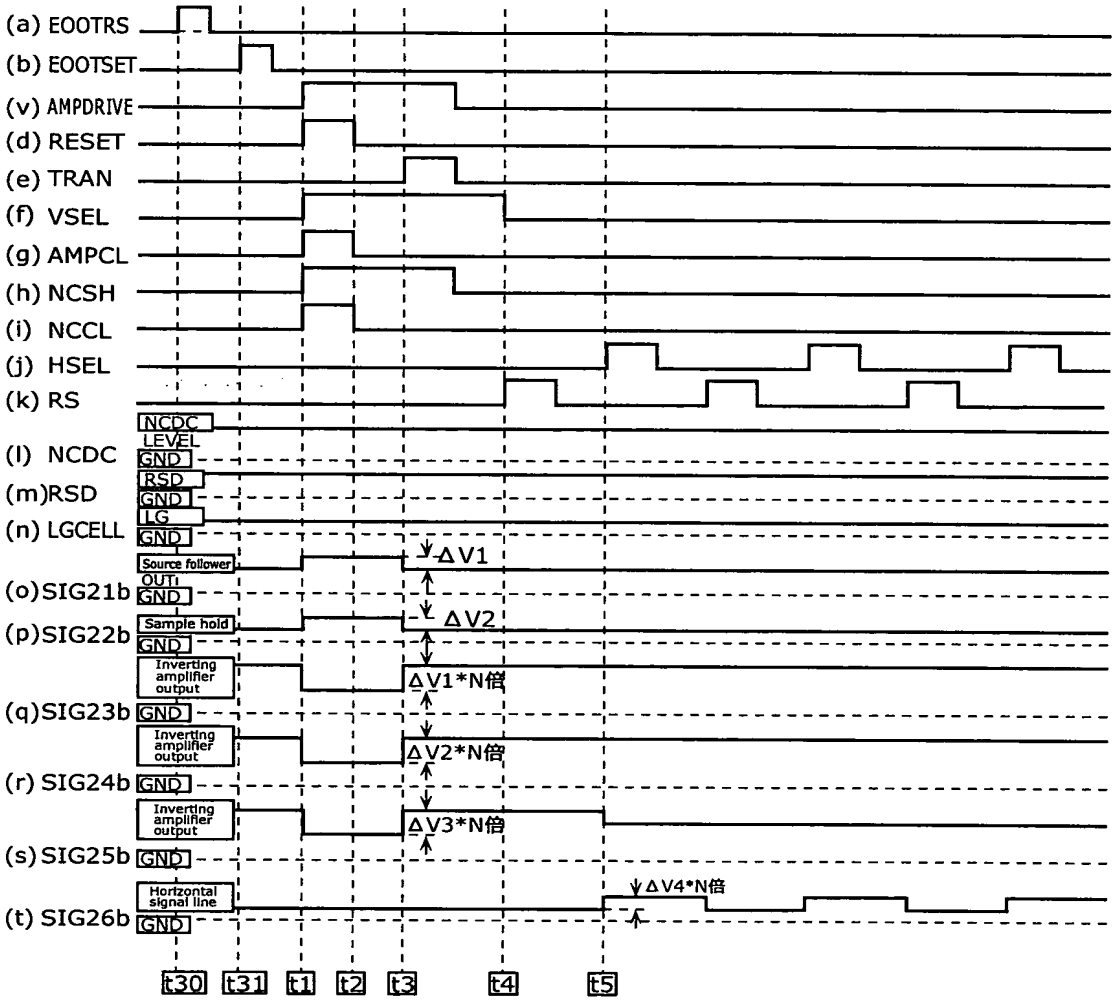

(a) EOOTRS
(b) EOOTSET
(v) AMPDRIVE
(d) RESET
(e) TRAN
(f) VSEL
(g) AMPCL
(h) NCSH
(i) NCCL
(j) HSEL
(k) RS
NCDC LEVEL
(l) NCDC
GND
RSD
(m)RSD
GND
LG
(n) LGCELL
GND
Source follower
OUT1
(o)SIG21b
GND
Sample hold
(p)SIG22b
GND
Inverting amplifier output
(q)SIG23b
GND
Inverting amplifier output
(r) SIG24b
GND
Inverting amplifier output
(s)SIG25b
GND
Horizontal signal line
(t) SIG26b
GND
ΔV1
ΔV2
ΔV1*N倍
ΔV2*N倍
ΔV3*N倍
ΔV4*N倍
t30
t31
t1
t2
t3
t4
t5

FIG. 17

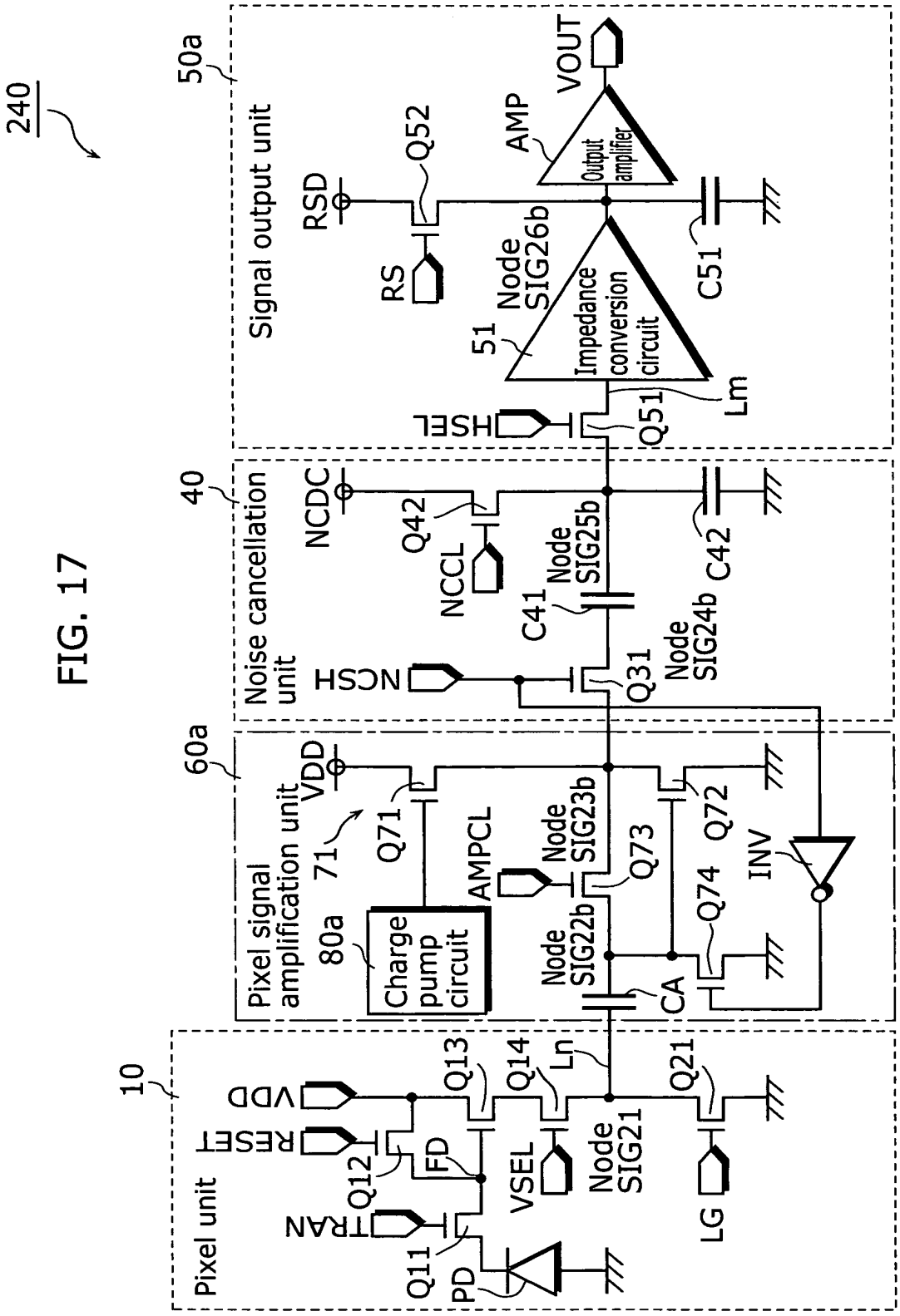

240
50a
Signal output unit
VOUT
AMP
Output amplifier
RSD
Q52
RS
Node SIG26b
51
Impedance conversion circuit
C51
HSEL
Q51
Lm
40
Noise cancellation unit
NCDC
Q42
NCCL
C41
Node SIG25b
C42
NCSH
Q31
Node SIG24b
60a
Pixel signal amplification unit
VDD
71
Q71
AMPCL
Node SIG23b
Q73
Q72
INV
80a
Charge pump circuit
Node SIG22b
CA
Q74
10
Pixel unit
VDD
RESET
Q12
FD
Q13
Q14
Ln
Q21
TRAN
Q11
PD
VSEL
Node SIG21
LG

FIG. 18

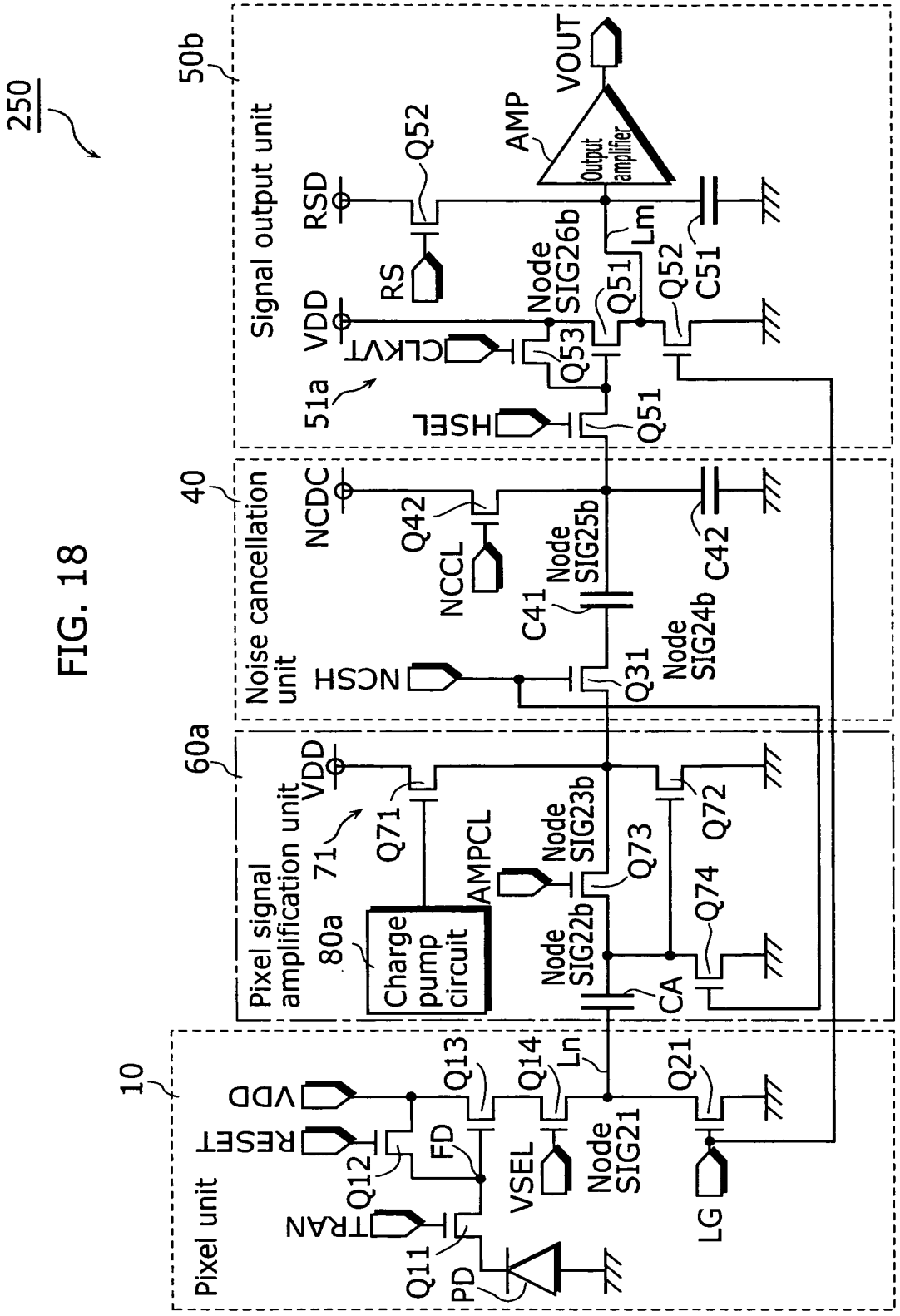

250
10
Pixel unit
VDD
RESET
TRAN
Q11
PD
Q12
FD
Q13
VSEL
Q14
Ln
Node SIG21
Q21
LG
60a
Pixel signal amplification unit
VDD
71
Q71
80a
Charge pump circuit
AMPCL
Node SIG23b
Q73
Node SIG22b
CA
Q74
Q72
40
Noise cancellation unit
NCDC
Q42
NCCL
C41
Node SIG25b
NCSH
Q31
Node SIG24b
C42
50b
Signal output unit
51a
VDD
CLKVT
HSEL
Q51
Q53
Node SIG26b
RS
RSD
Q52
AMP
Output amplifier
VOUT
Lm
Q51
Q52
C51

FIG. 19

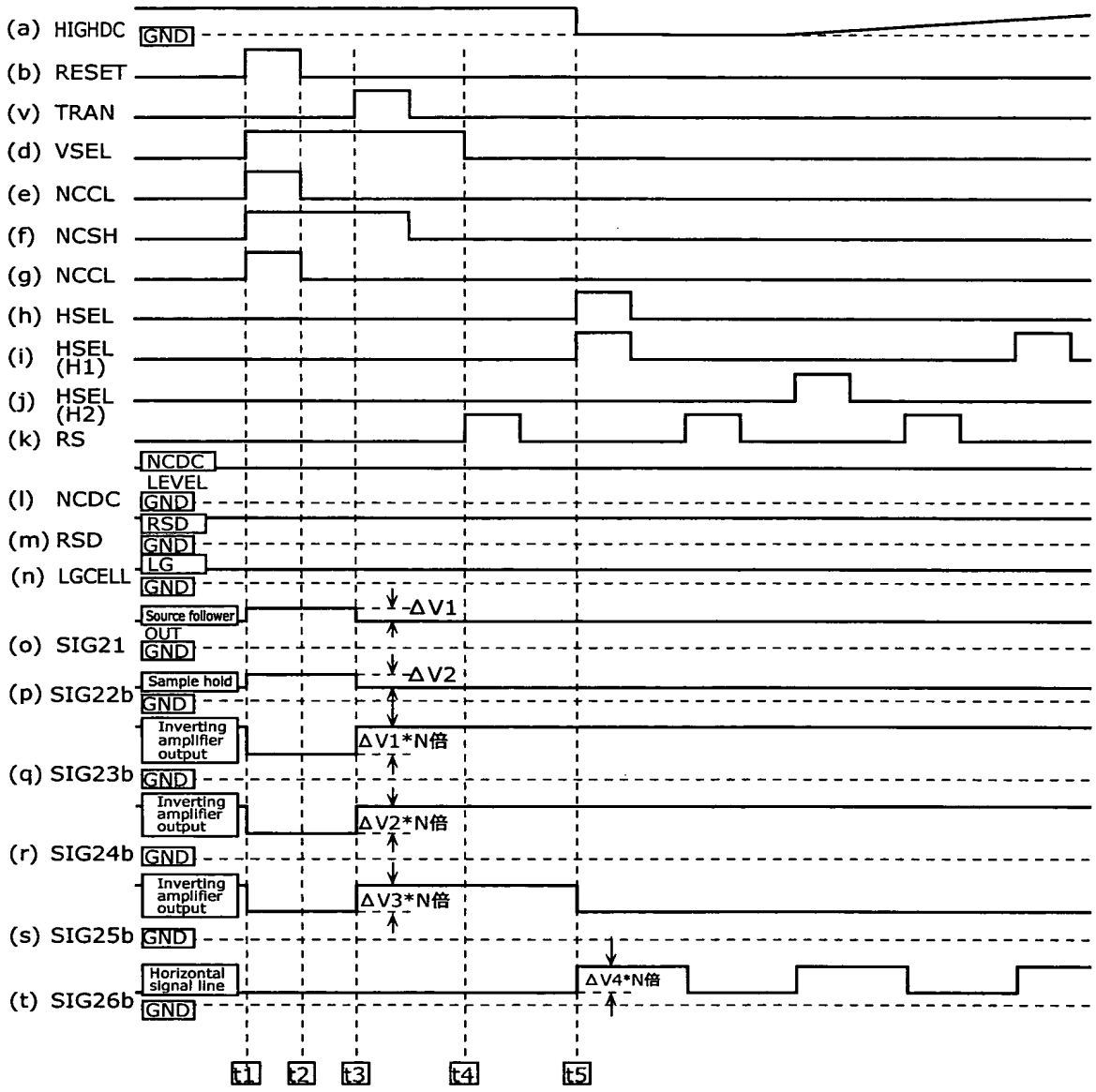

(a) HIGHDC
GND
(b) RESET
(v) TRAN
(d) VSEL
(e) NCCL
(f) NCSH
(g) NCCL
(h) HSEL
(i) HSEL (H1)
(j) HSEL (H2)
(k) RS
NCDC LEVEL
(l) NCDC
GND
RSD
(m) RSD
GND
LG
(n) LGCELL
GND
Source follower OUT
-ΔV1
(o) SIG21
GND
Sample hold
-ΔV2
(p) SIG22b
GND
Inverting amplifier output
ΔV1*N倍
(q) SIG23b
GND
Inverting amplifier output
ΔV2*N倍
(r) SIG24b
GND
Inverting amplifier output
ΔV3*N倍
(s) SIG25b
GND
Horizontal signal line
ΔV4*N倍
(t) SIG26b
GND
t1
t2
t3
t4
t5

FIG. 20

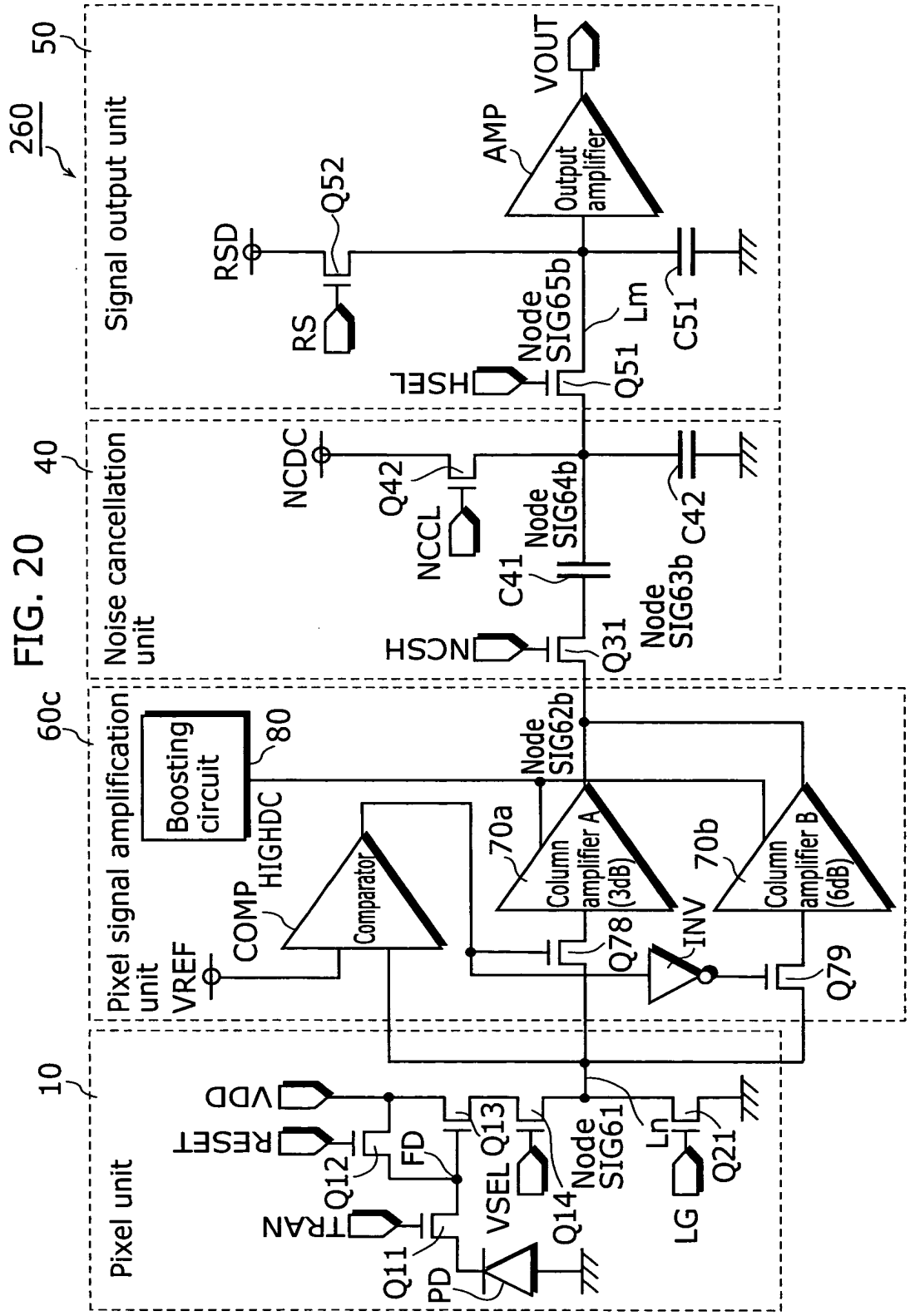
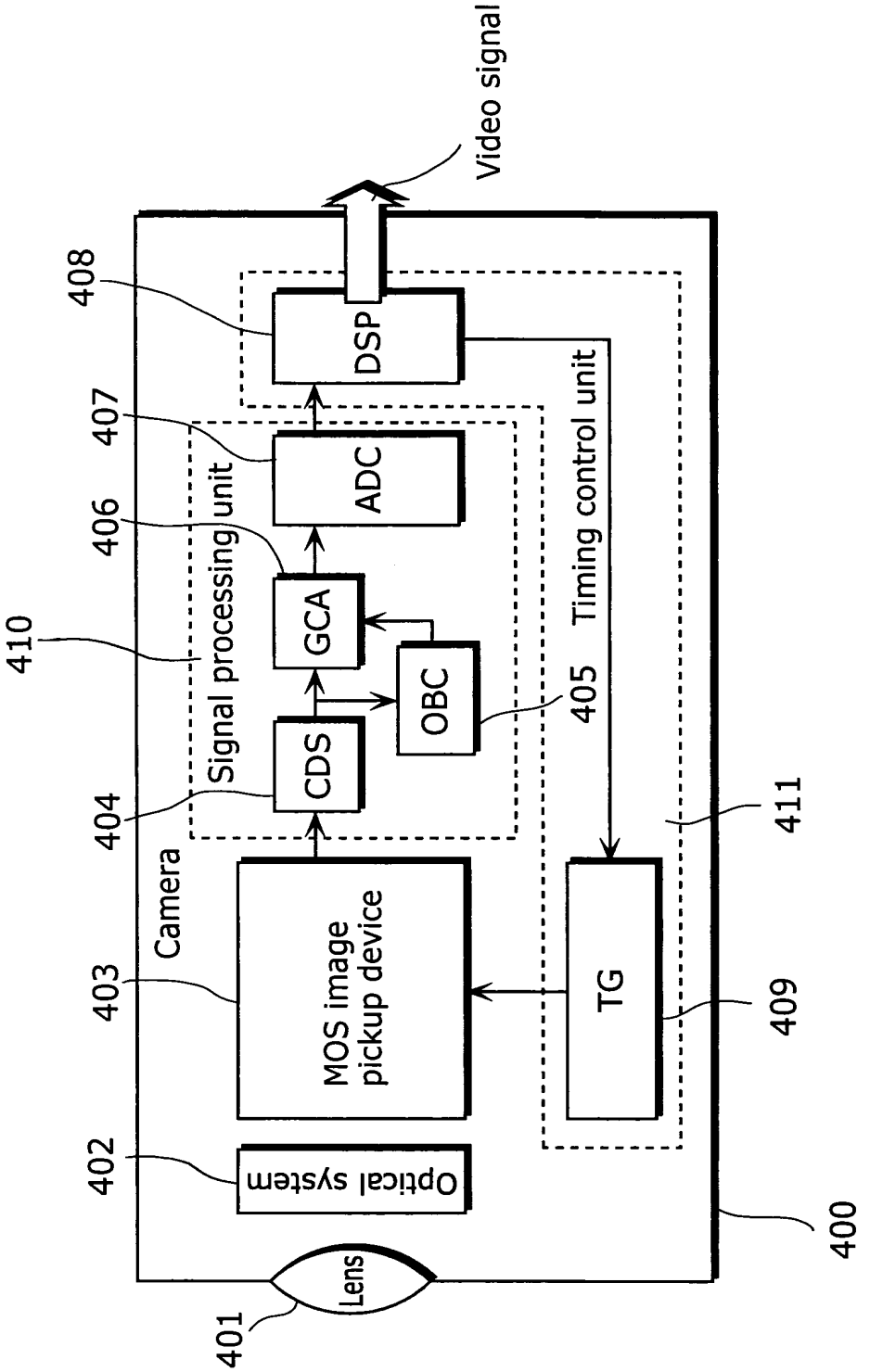

260
50
Signal output unit
VOUT
AMP
Output amplifier
RSD
Q52
RS
HSEL
Node SIG65b
Q51
Lm
C51
40
Noise cancellation unit
NCDC
Q42
NCCL
Node SIG64b
C41
C42
NCSH
Q31
Node SIG63b
60c
Pixel signal amplification unit
Boosting circuit
80
Node SIG62b
VREF
COMP
HIGHDC
Comparator
70a
Column amplifier A (3dB)
INV
70b
Column amplifier B (6dB)
Q78
Q79
10
Pixel unit
VDD
RESET
Q12
FD
Q13
TRAN
Q11
PD
VSEL
Q14
Node SIG61
Ln
Q21
LG

FIG. 21


Video signal
408
DSP
407
ADC
406
GCA
410
Signal processing unit
OBC
405
Timing control unit
404
CDS
411
Camera
403
MOS image pickup device
TG
409
402
Optical system
400
Lens
401